a depressed region having an edge portion being depressed beyond said ordinary region due to presence of said concave part,

said at least one MOS transistor includes:

a first MOS transistor being formed on said depressed region, and

a second MOS transistor being formed on said ordinary region, and

a length of a margin part of a first gate electrode constructing said first MOS transistor in said depressed region is set to be larger than that of a margin part of a second gate electrode constructing said second MOS transistor in said ordinary region, wherein a length of the margin part of the second gate electrode is X, the length of the margin part of the first gate electrode is $X + \alpha$ where $0 < \alpha \leq X$, wherein

said concave part is formed on a corner portion of said active area, and

the length of said margin part of said first gate electrode is set at the total of the length of said margin part of said second gate electrode and a length being equal to a depression length in said concave part.

3. (Amended) A semiconductor device comprising:

an active area being provided with at least one MOS transistor; and

an insulating film defining said active area, wherein

said active area is set in a shape having a concave part in a shape along a plan view,

said active area is provided with:

an ordinary region, and

a depressed region having an edge portion being depressed beyond said ordinary region due to presence of said concave part,

said at least one MOS transistor includes:

a first MOS transistor being formed on said depressed region, and

a second MOS transistor being formed on said ordinary region, and

a length of a margin part of a first gate electrode constructing said first MOS transistor in said depressed region is set to be larger than that of a margin part of a second gate electrode constructing said second MOS transistor in said ordinary region, wherein a length of the margin part of the second gate electrode is X, the length of the margin part of the first gate electrode is $X + \alpha$ where $0 < \alpha \leq X$, wherein

said concave part is formed on a corner portion of said active area, and

the length of said margin part of said first gate electrode is set at the total of:

the length of said margin part of said second gate electrode, and

the length of a portion between said edge portion of said depressed region and an intersection between a virtual line being set to connect first and second convex corner portions of said active area in said concave part and said first gate electrode.

13. (New) A semiconductor device comprising:

an active area with at least one MOS transistor to be formed therein; and

an insulation film for defining said active area,

said active area having a recess in plan configuration,

said recess being defined by first, second and third edges,

said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend,

said active area having a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

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said at least one MOS transistor including

a first MOS transistor having a first gate electrode, and

a second MOS transistor having a second gate electrode,

said first gate electrode extending in a direction perpendicular to the direction in which said fourth edge extends, said first gate electrode having a first end extending beyond said fourth edge over said insulation film,

said second gate electrode extending in a direction perpendicular to the direction in which said third edge extends, said second gate electrode having a first end extending beyond said third edge over said insulation film,

said first gate electrode having a first length from said fourth edge to said first end thereof, said second gate electrode having a second length from said third edge to said first end thereof, said second length being greater than said first length.

14. (New) The semiconductor device according to claim 13, wherein said first edge is greater in length than said second edge, and said second length is greater than at least the length of said second edge.

15. (New) The semiconductor device according to claim 14, wherein said second length is a sum of said first length and the length of said second edge.

16. (New) The semiconductor device according to claim 14, wherein said second length is a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

17. (New) The semiconductor device according to claim 13, wherein said second length is greater than the lengths of said first and second edges.

18. (New) The semiconductor device according to Claim 17, wherein said first and second gate electrodes are parallel to each other, and said first end of said first gate electrode and said first end of said second gate electrode are in a line.

19. (New) A method of manufacturing a semiconductor device including an active area with at least one MOS transistor to be formed therein, and an insulation film for defining said active area, based on layout design comprising the steps of:

(a) configuring said active area to have a recess in plan configuration; and

(b) configuring a first MOS transistor having a first gate electrode and a second MOS transistor having a second gate electrode on said active area,

said step (a) including the steps of

configuring said recess to be defined by first, second and third edges, said first and second edges being parallel to each other, with said insulation film positioned therebetween,

said third edge being connected to a first end of said first edge and a first end of said second edge, said third edge extending in a direction perpendicular to a direction in which said first and second edges extend, and

configuring a fourth edge connected to a second end opposite from said first end of said first edge, said fourth edge being parallel to said third edge, said fourth edge extending in a direction opposite from said second edge,

said step (b) including the steps of

configuring said first gate electrode to extend in a direction perpendicular to the direction in which said fourth edge extends and to have a first and end extending beyond said fourth edge over said insulation film, and

configuring said second gate electrode to extend in a direction perpendicular to the direction in which said third edge extends and to have a first end extending beyond said third edge over said insulation film,

said first gate electrode having a first length from said fourth edge to said first end thereof, said second gate electrode having a second length from said third edge to said first end thereof, said second length being greater than said first length.

20. (New) The method according to claim 19, wherein

said step (a) includes configuring said first edge to be greater in length than said second edge, and

said step (b) includes configuring said second length to be greater than at least the length of said second edge.

21. (New) The method according to claim 20, wherein

said step (b) includes configuring said second length to equal a sum of said first length and the length of said second edge.

22. (New) The method according to claim 20, wherein

said step (b) includes configuring said second length to equal a sum of said first length and a length from said third edge to an intersection of said second gate electrode and an imaginary line connecting said second end of said first edge and a second end of said second edge.

23. (New) The method according to claim 19, wherein said step (b) includes configuring said second length to be greater than the lengths of said first and second edges.

24. (New) The method according to claim 23, wherein said step (b) includes

configuring said first and second gate electrodes to be parallel to each other, and

configuring said first end of said first gate electrode and said first end of said second gate electrode to be in a line.